Chapter 9

Built-In-Self-Test

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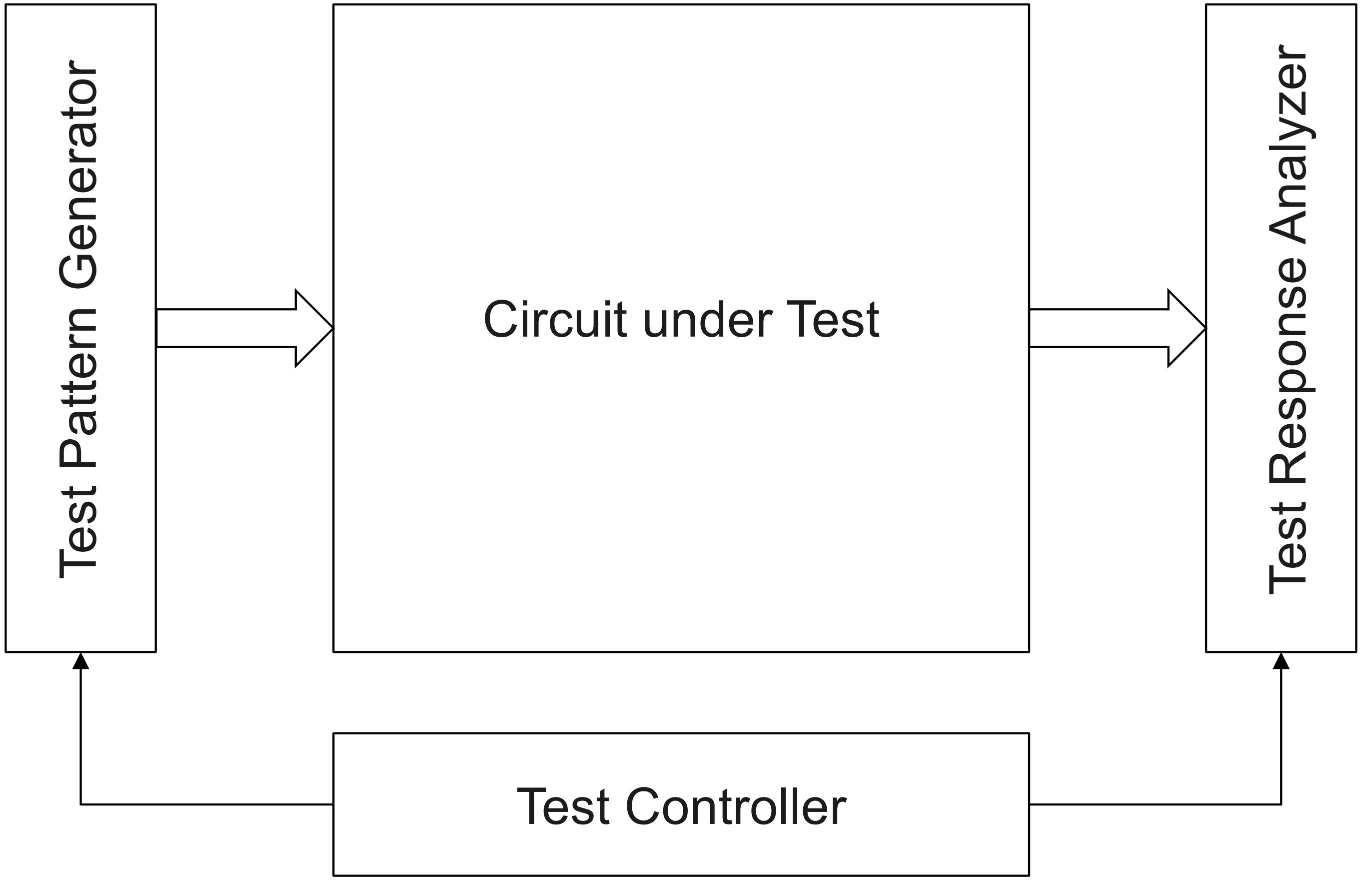
Why?

- High and ever-increasing price of ATE
- Long and difficult test sequence generations high sequence
- Accessibility problem in complex SoC
- On-site test necessity due to the application

BIST Principle



Advantages

- Eliminate the need for an expensive ATE
- Possibility of nominal speed testing
- Good and "flexible" coverage rate
- Short test time (speed + prioritization)
- Possibility of in-site test (dormancy time)

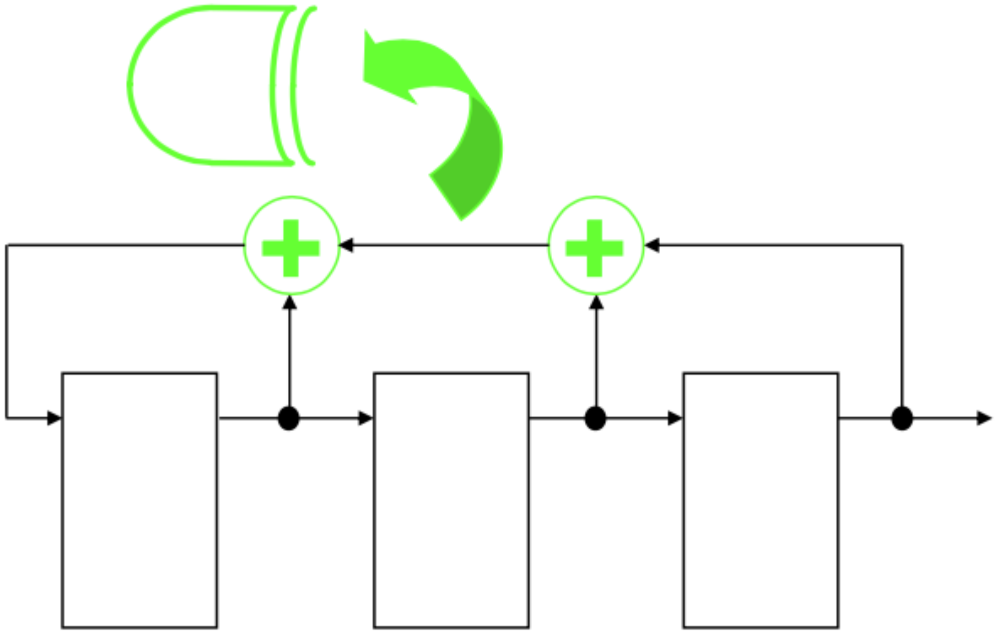
Outline

- Integrated test vector generation
- Integrated response analysis
- BIST structures
- BIST planification and controlling

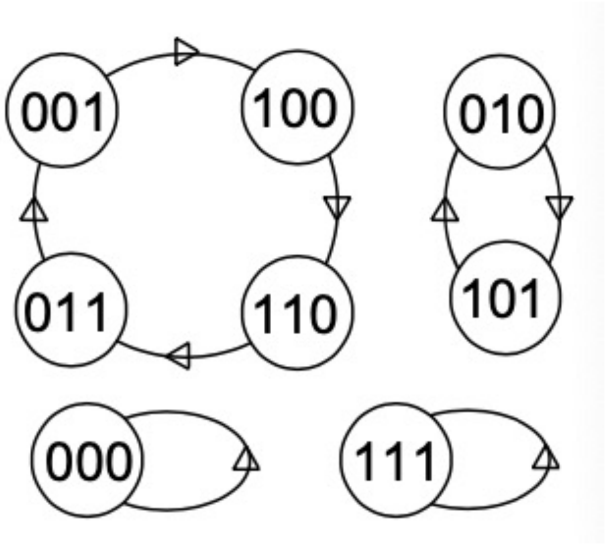
Test Vector Generation

- Radom Testing (pseudo-random)
  - no need for ATPG
  - long test (TC depending on the length of the sequence)
  - pseudo-random: same characteristic as random but applied deterministically
- Deterministic Testing
  - use of ATPG
  - fixed and optimal vectors
- Exhaustive Testing (pseudo-exhaustive)
  - no need for ATPG
  - pseudo-exhaustive: same characteristic as exhaustive but shorter sequence

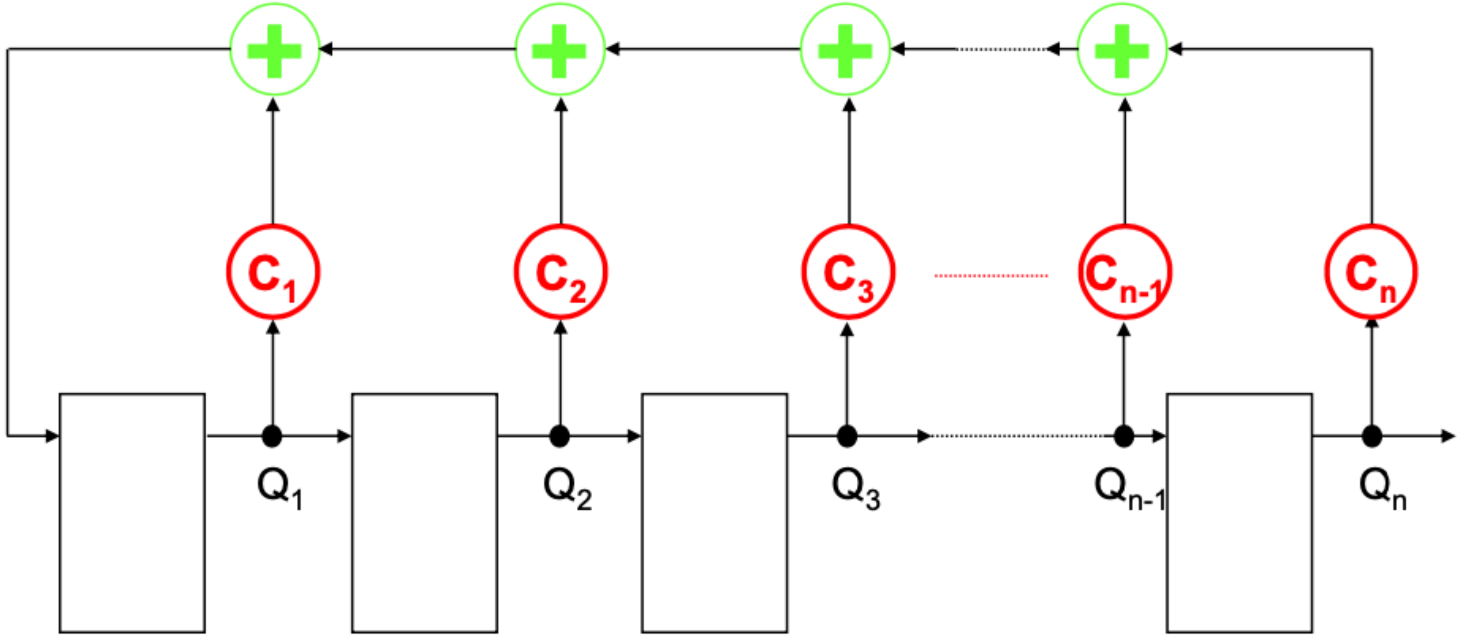
LFSR



The sequence of states generated always depends on the initial state



Generalization

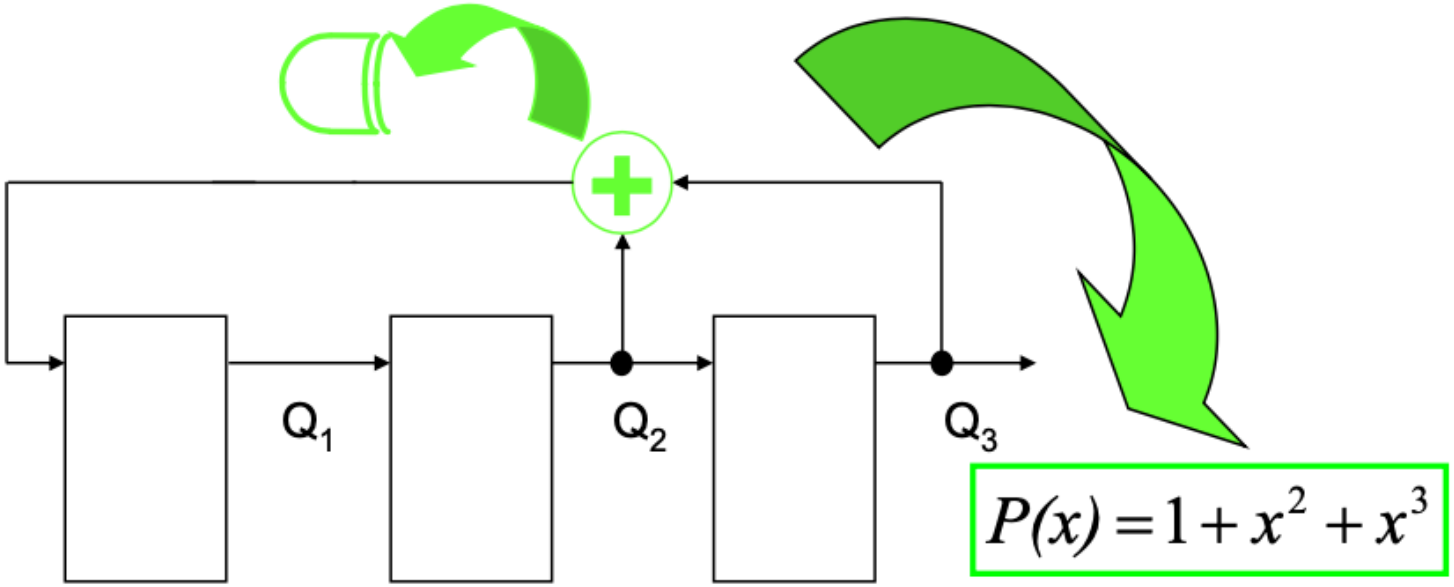


c_i=1 if the connexion exists otherwise $c_i = 0$

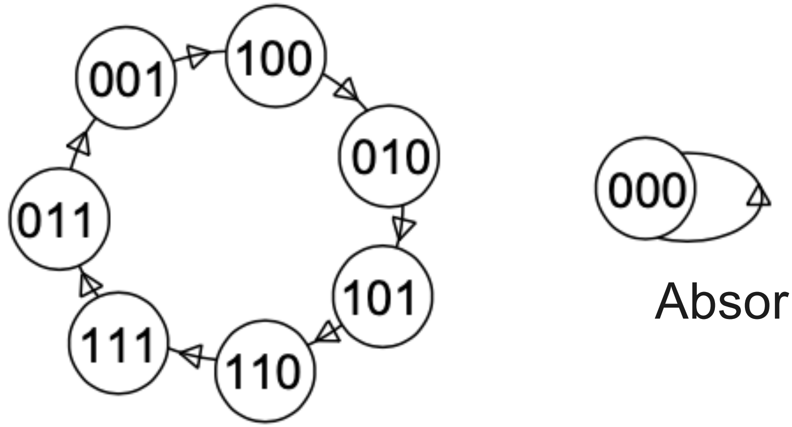
Generalization

- For an LFSR of n flip-flops, a sequence of length 2^n-1 is said to be of maximum length
- The characteristic polynomial of a maximum length LFSR is called a primitive polynomial
- There are primitive polynomials for all values of n
- In practice we favor primitive polynomials with few terms (smaller surface)

LFSR with n=3



$$P(x) = 1 + x^2 + x^3$$

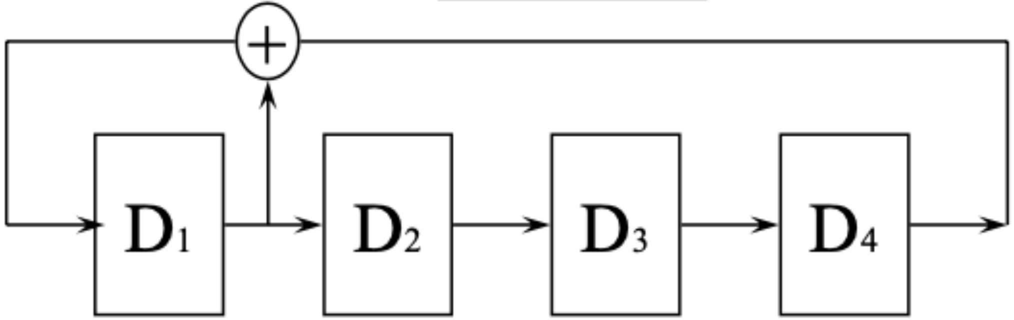


Maximal length sequence

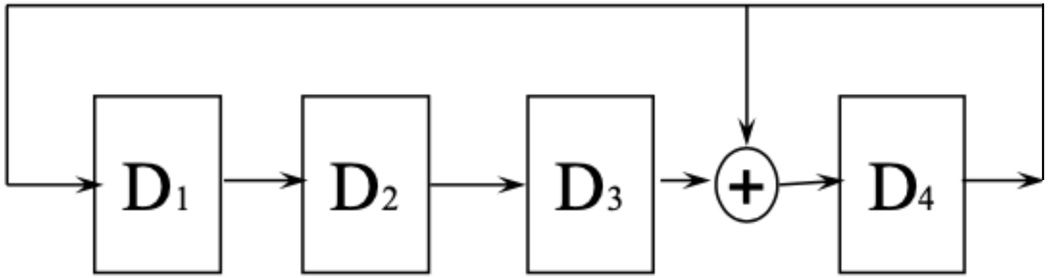
Absorbing state

LFSR Types

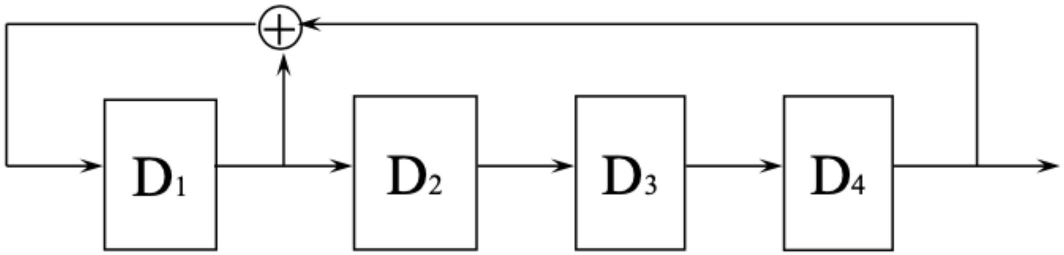
Type 1



Type 2



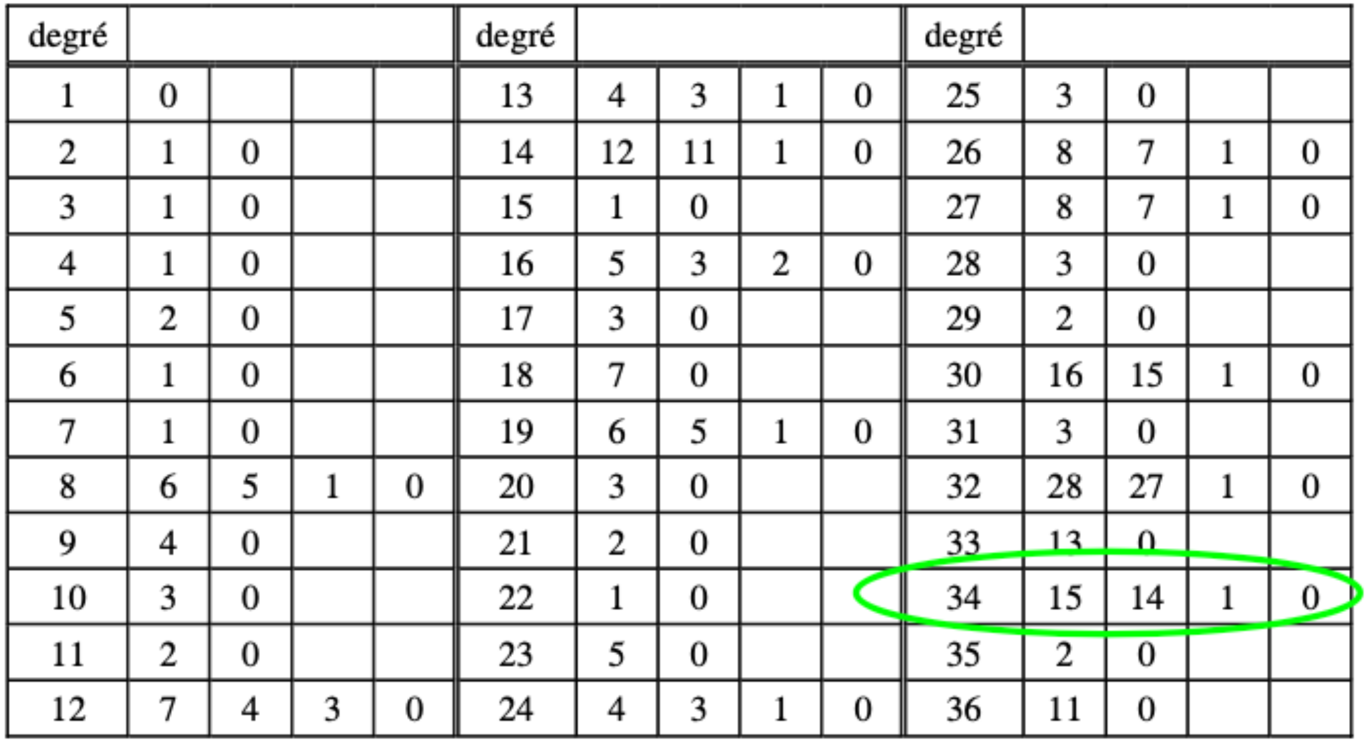
LFSR Type 1 with n=4



$$g(x) = x^4 + x^1 + 1$$

D1	D2	D3	**D4**
0	0	0	1
1	0	0	0
1	1	0	0
1	1	1	0
1	1	1	1
0	1	1	1
1	0	1	1
0	1	0	1
1	0	1	0
1	1	0	1
0	1	1	0
0	0	1	1
1	0	0	1
0	1	0	0
0	0	1	0
0	**0**	**0**	**1**

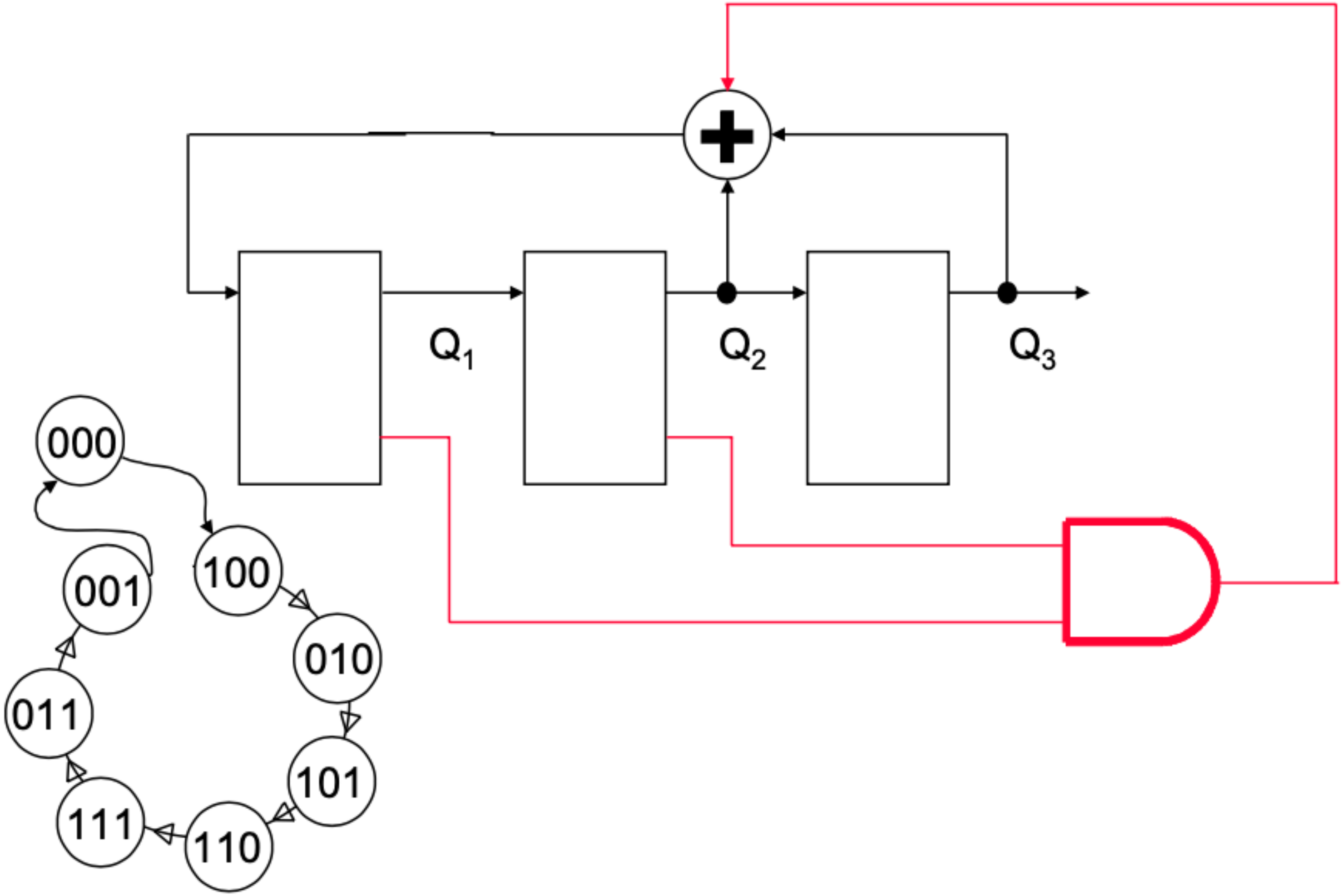
Some Primitive Polynomial



degré					degré					degré				
1	0				13	4	3	1	0	25	3	0		
2	1	0			14	12	11	1	0	26	8	7	1	0
3	1	0			15	1	0			27	8	7	1	0
4	1	0			16	5	3	2	0	28	3	0		
5	2	0			17	3	0			29	2	0		
6	1	0			18	7	0			30	16	15	1	0
7	1	0			19	6	5	1	0	31	3	0		
8	6	5	1	0	20	3	0			32	28	27	1	0
9	4	0			21	2	0			33	13	0		
10	3	0			22	1	0			34	15	14	1	0
11	2	0			23	5	0			35	2	0		
12	7	4	3	0	24	4	3	1	0	36	11	0		

$$\boxed{P(x) = x^{34} + x^{15} + x^{14} + x + 1}$$

Exhaustive Generation

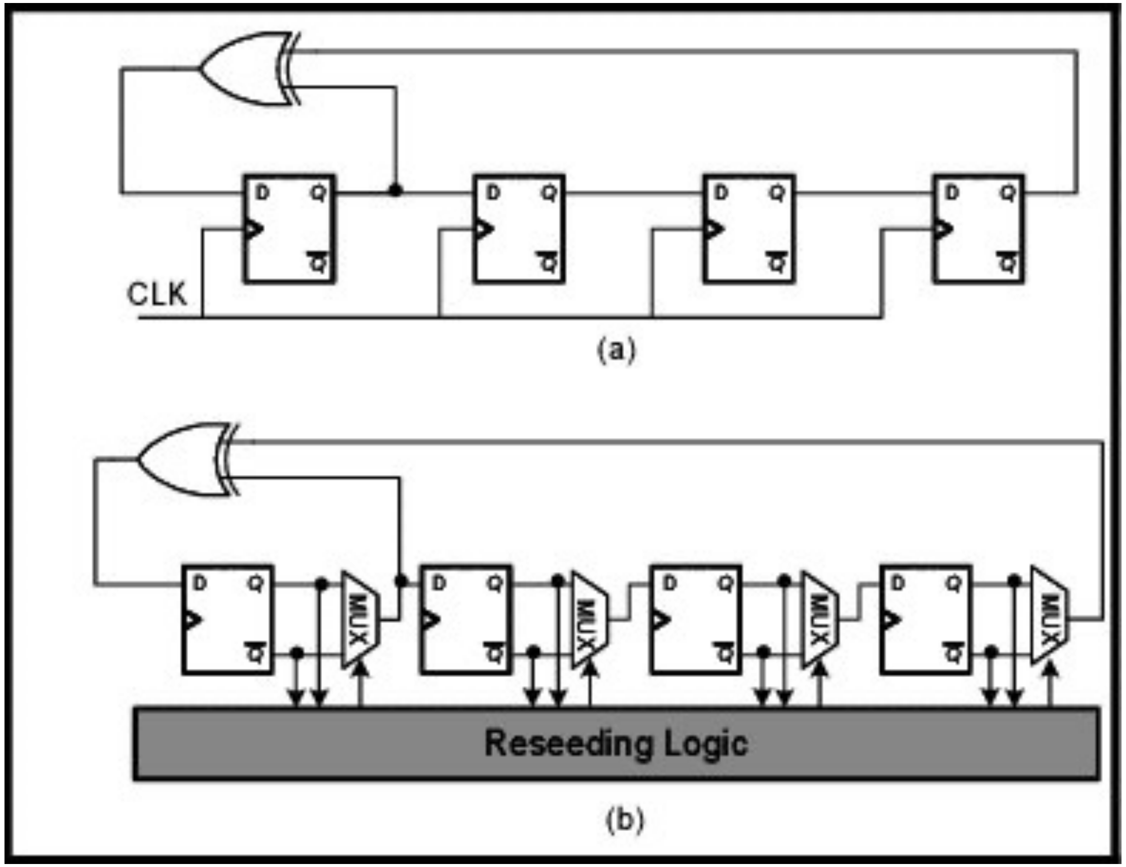


Deterministic Generation

- Generation of a test sequence by ATPG
- Generation of this sequence by a hardware structure
  - ROM: simple but expensive
  - FSM: still simple but still expensive
  - Research in progress

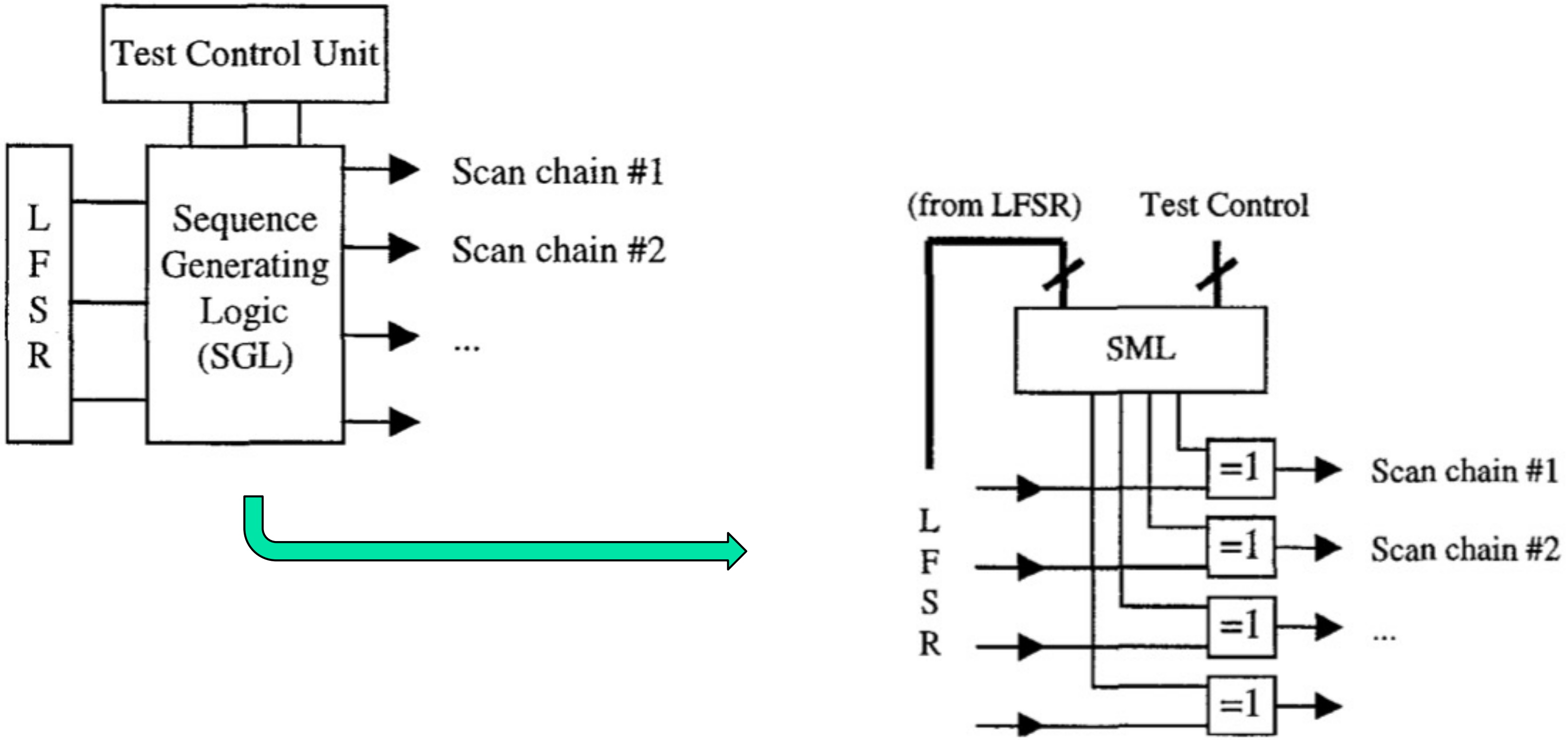
LFSR Reseeding

- Idea: Regularly change the state of the LFSR



Deterministic BIST

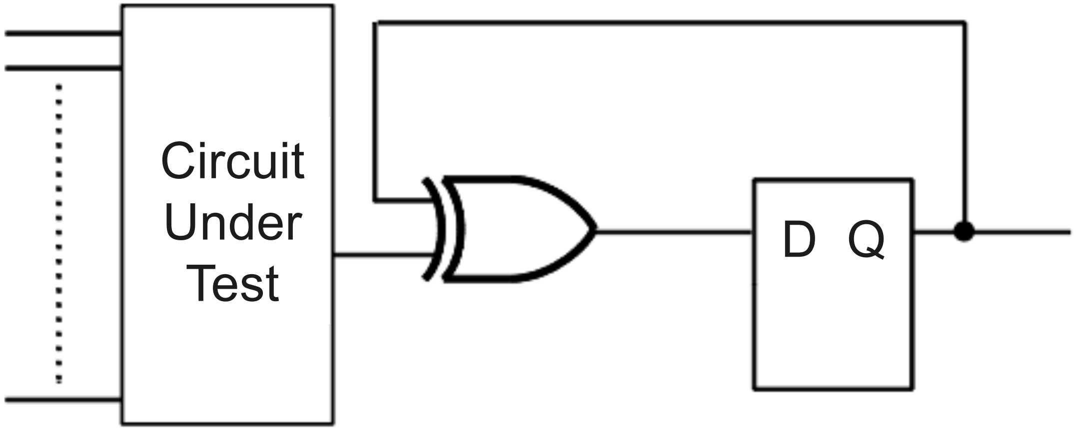
- Idea: Reproduce the deterministic test vectors



Integrated Response Analysis

- Parity check
- Response compaction by counting
    - counting of 1 (0)
    - counting of transitions
- Response compaction using a LFSR

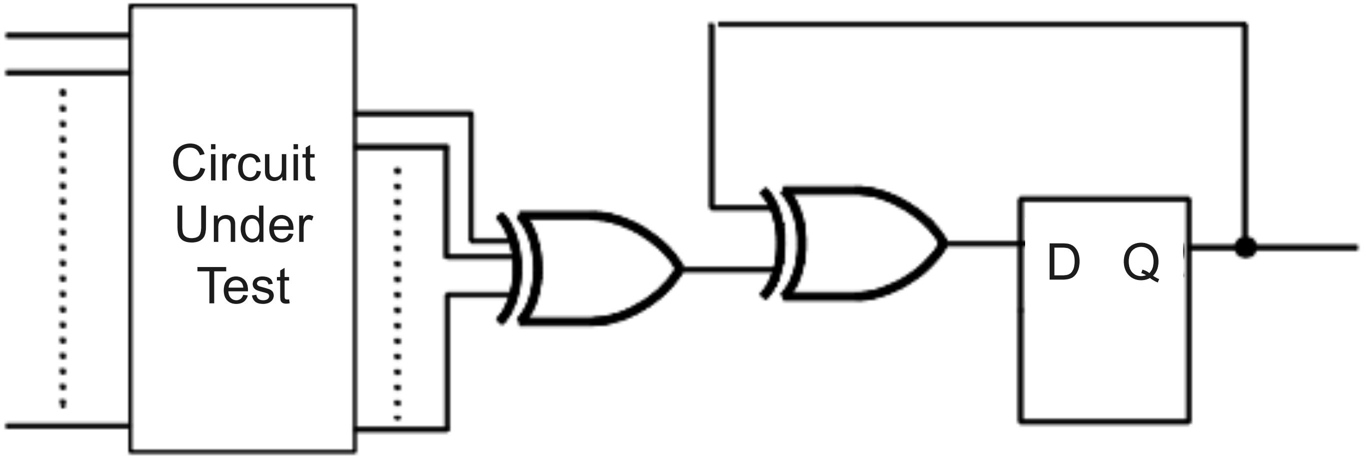
Parity Check



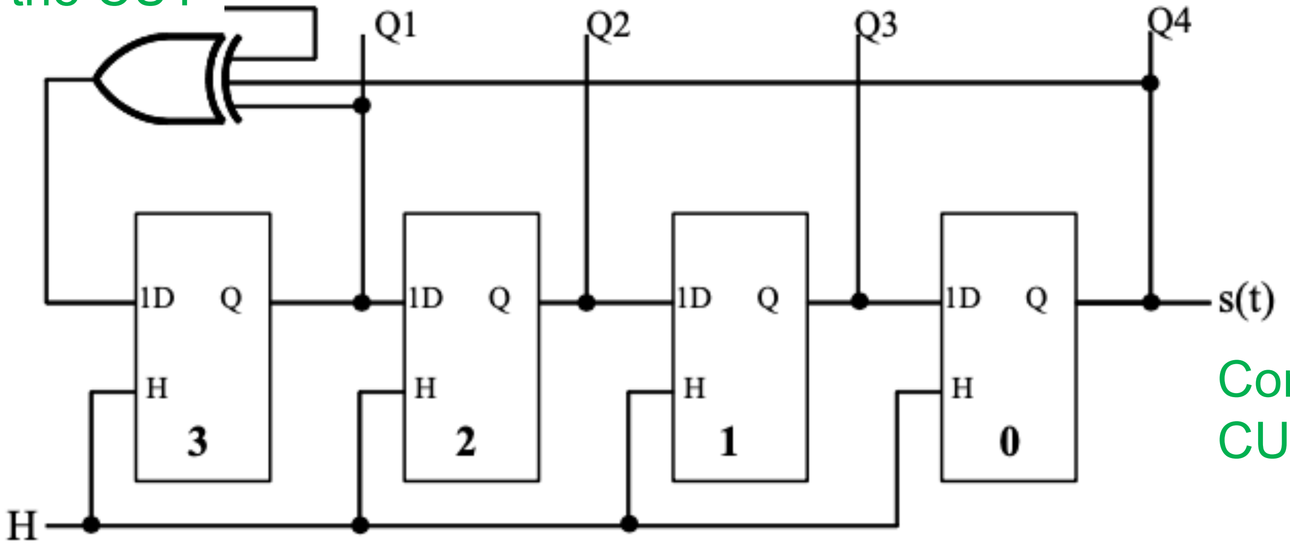
- FF initialization
- Sum over x cycles (mod 2) of the output
- Detection of simple one-bit errors and odd-numbered errors on a string of m bits
- Masking probability $P_m = \dfrac{\frac{2^m}{2} - 1}{2^m - 1}$

With more than one output

- Associate a parity checker at each output
    - high cost
- Groupe the outputs before compression
    - higher masking rate



Compaction using a LFSR



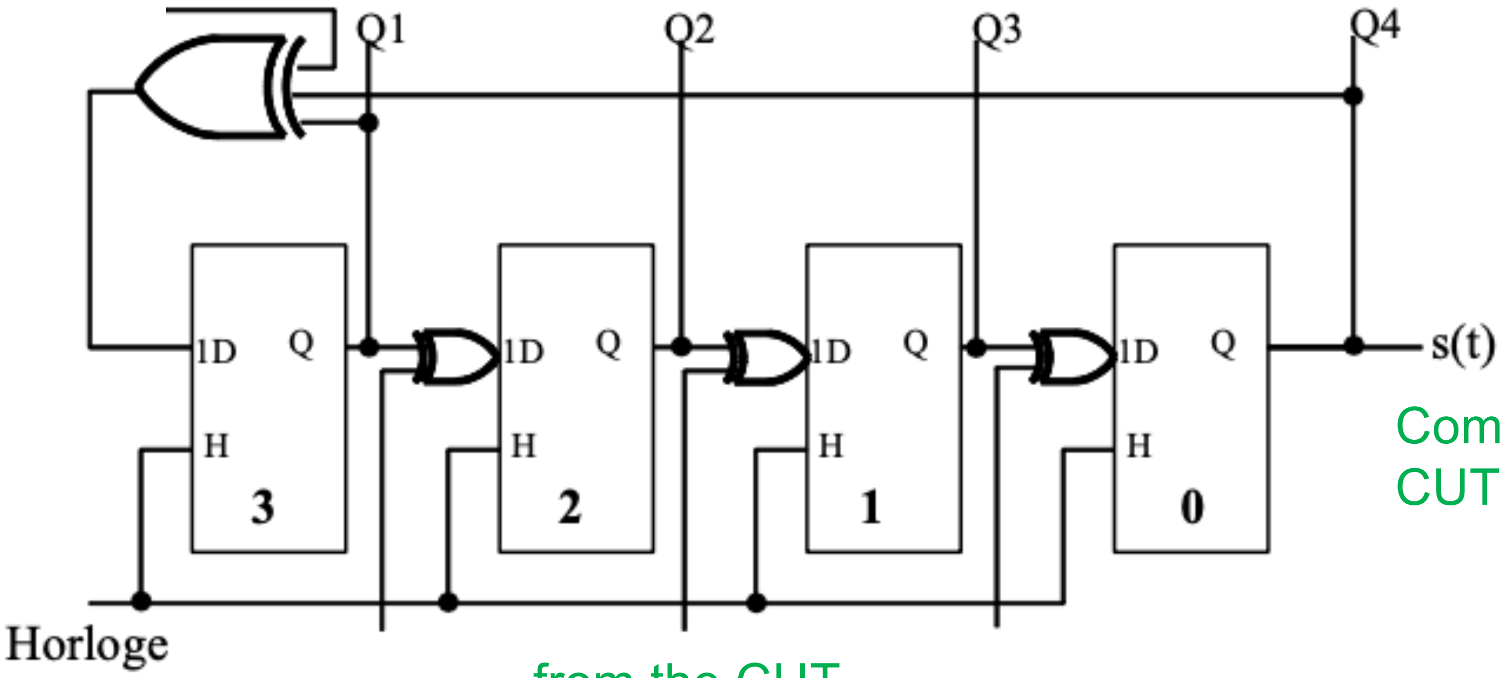
Compacted
CUT response

- Low masking rate and "flexible"

$$Pm = \frac{1}{2^n}$$

with n the number of flip-flops

Compaction using a MISR



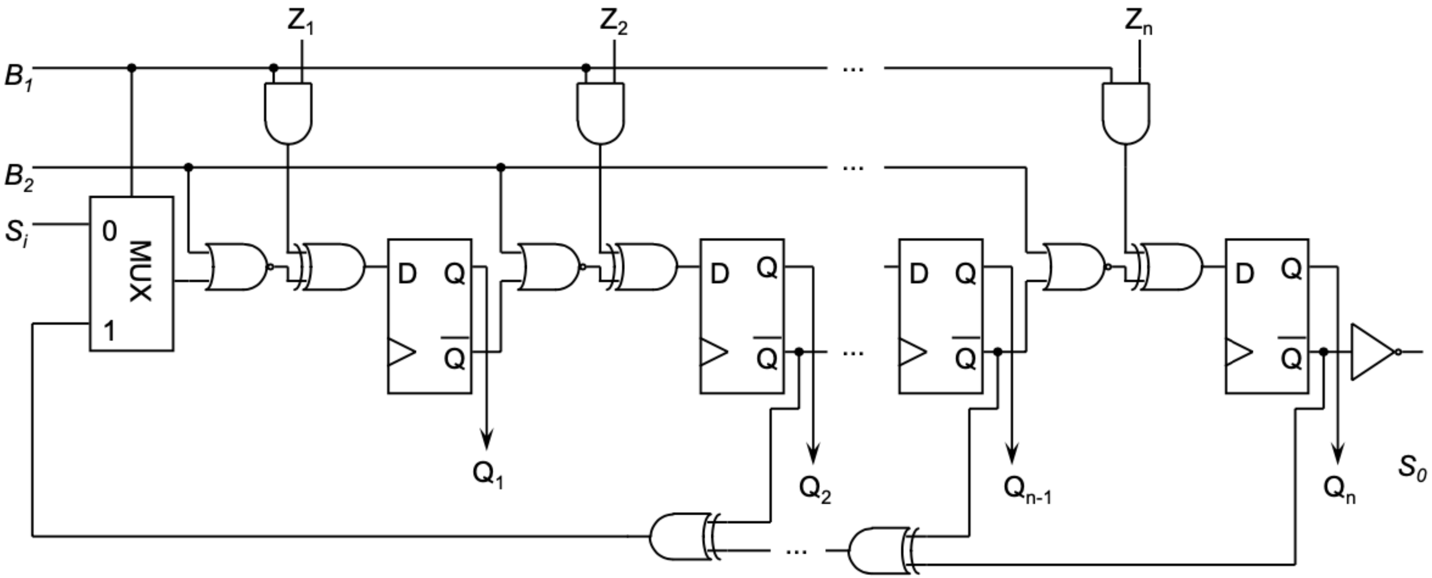
from the CUT

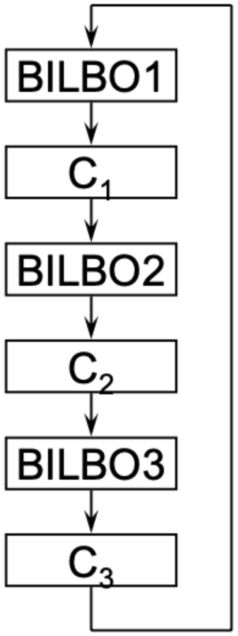
from the CUT

Compacted CUT response

BILBO

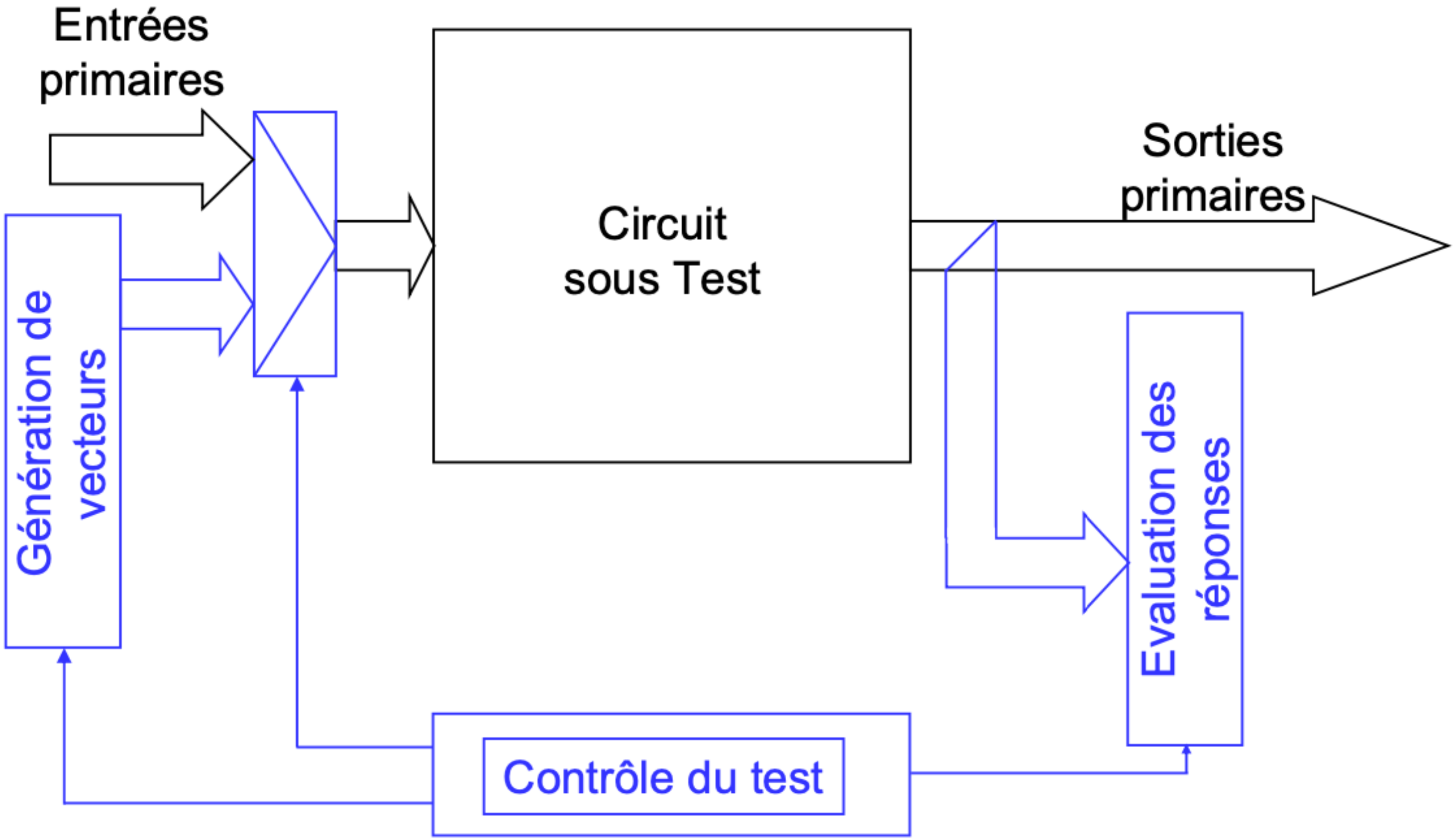
- Built-In Logic Block Observation





B_1	B_2	BILBO
0	0	shift register
0	1	reset
1	0	MISR (input * constant * LFSR)
1	1	parallel load (normal operation)

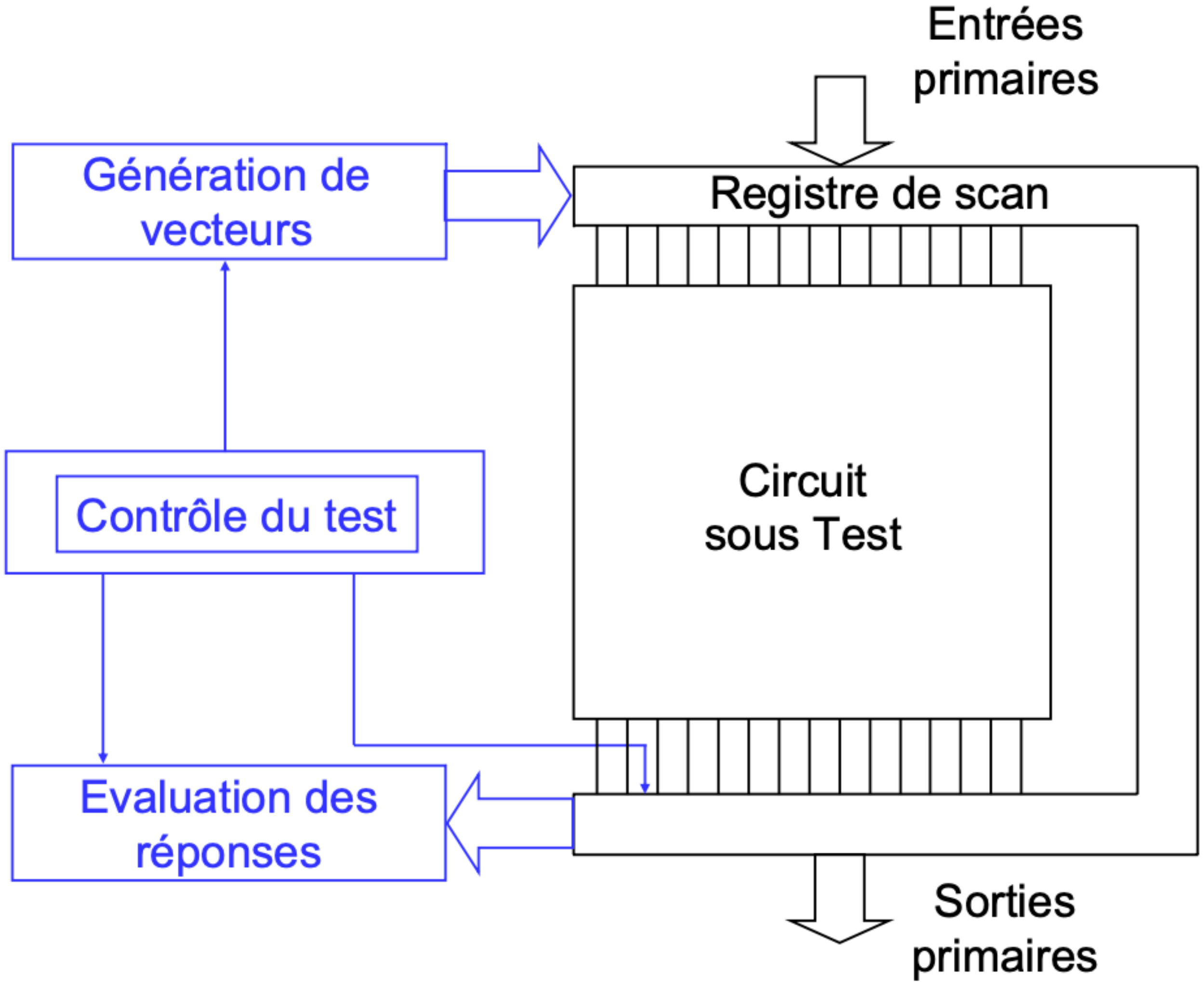
Test per Clock



Pros and Cons

- Pros
  - Reduced test time
  - At speed testing
- Cons
  - Area cost due BILBO registers
  - Complexity of the control part
  - Performance penalty due to the insertion of test registers

Test per Scan



Pros and Cons

- Pros
    - Suitable for any commercial design flow
    - Low performance penalty since the BIST hardware is external
    - The control of the BIST is simple
    - Extendable to partial scan and multiple scan
- Cons
    - Long test time (serial input)
    - *At speed test not allowed*